



## Electrical Specifications: $T_A = 25^\circ\text{C}^1$

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Reference Insertion Loss	—	DC - 0.5 GHz	dB	—	3.5	3.8
		DC - 1.0 GHz	dB	—	3.9	4.2
		DC - 2.0 GHz	dB	—	4.2	4.6
Attenuation Accuracy <sup>2</sup>	Any Single Bit Any Combination of Bits (For attenuation to 26 dB) Any Combination of Bits (For attenuation 27 to 50 dB)	DC - 2.0 GHz	dB	± (0.3 +4% of atten. setting)		
		DC - 2.0 GHz	dB	± (0.4 +4% of atten. setting)		
		DC - 1.5 GHz	dB	± (0.5 +5% of atten. setting)		
VSWR	—	0.05 - 0.10 GHz 0.101 - 2.0 GHz	Ratio Ratio	— —	— —	2.0:1 1.8:1
Trise, Tfall	10% to 90%	—	ns	—	—	50
Ton, Toff	50% Control to 90/10% RF	—	ns	—	—	150
Transients	In-Band (peak-peak)	—	mV	—	50	—
1 dB Compression	Input Power Input Power	0.05 GHz	dBm	—	+20	—
		0.5 - 2.0 GHz	dBm	—	+28	—
Input IP3	For two-tone Input Power Up to +5 dBm	0.05 GHz	dBm	—	+34	—
		0.5 - 2.0 GHz	dBm	—	+46	—
Input IP2	For two-tone Input Power Up to +5 dBm	0.05 GHz	dBm	—	+45	—
		0.5 - 2.0 GHz	dBm	—	+79	—
Vcc	—	—	V	4.5	5.0	5.5
Vee	—	—	V	-8.0	—	-5.0
Icc	Vcc = 4.5 to 5.5V Vctl = 0 to 0.8V, or Vcc – 2.1V to Vcc	—	mA	—	—	6.0
Iee	Vee = -5.0 to -8.0V	—	mA	—	—	1.0

1. All specifications apply when operated with bias voltages of +5V for Vcc and –5.0V for Vee.
2. This attenuator is guaranteed monotonic.

## Absolute Maximum Ratings <sup>3,4</sup>

Parameter	Absolute Maximum
Max Input Power 0.05 GHz 0.5 - 2.0 GHz	+27 dBm +34 dBm
$V_{CC}$	$-0.5V \leq V_{CC} \leq +7.0V$
$V_{EE}$	$-8.5V \leq V_{EE} \leq +0.5V$
$V_{CC} - V_{EE}$	$-0.5V \leq V_{CC} - V_{EE} \leq 14.5V$
$V_{in}^5$	$-0.5V \leq V_{in} \leq V_{CC} + 0.5V$
Operating Temperature	$-40^{\circ}C$ to $+125^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

## Handling Procedures

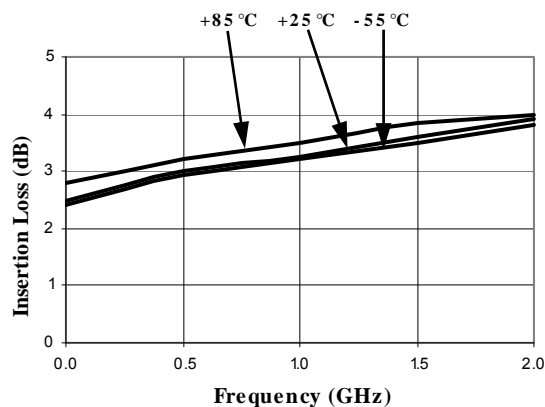
Please observe the following precautions to avoid damage:

## Static Sensitivity

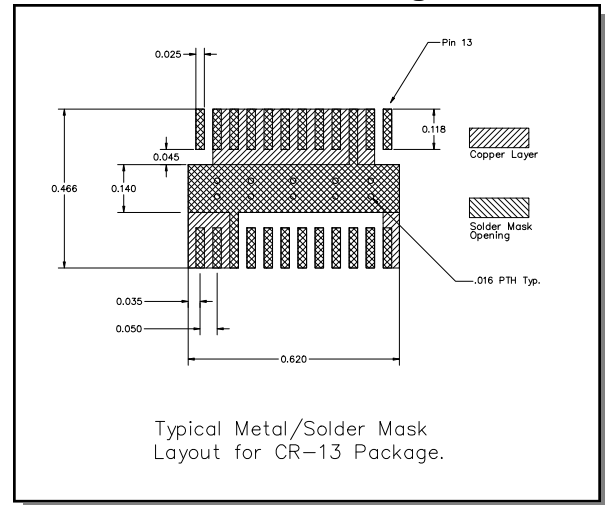
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

## Typical Performance Curves

### Insertion Loss vs. Frequency



## Recommended PCB Configuration

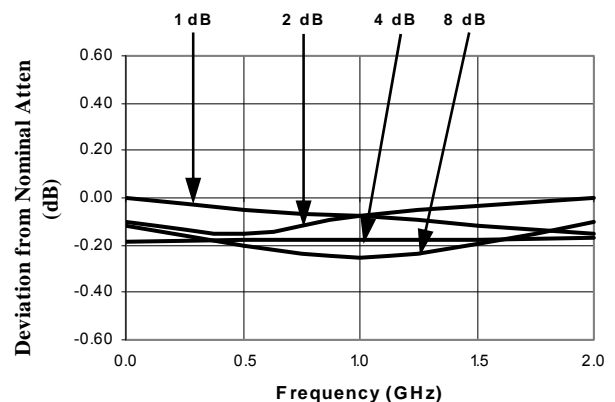


## Truth Table (Digital Attenuator)

Control Inputs						Attenuation
C6	C5	C4	C3	C2	C1	
0	0	0	0	0	0	Reference
0	0	0	0	0	1	1 dB
0	0	0	0	1	0	2 dB
0	0	0	1	0	0	4 dB
0	0	1	0	0	0	8 dB
0	1	0	0	0	0	16 dB
1	0	0	0	0	0	32 dB
1	1	1	1	1	1	63 dB

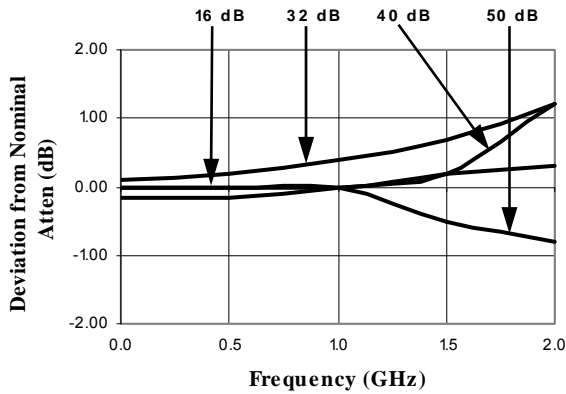
0 = TTL Low; 1 = TTL High

### Attenuation Accuracy vs. Frequency

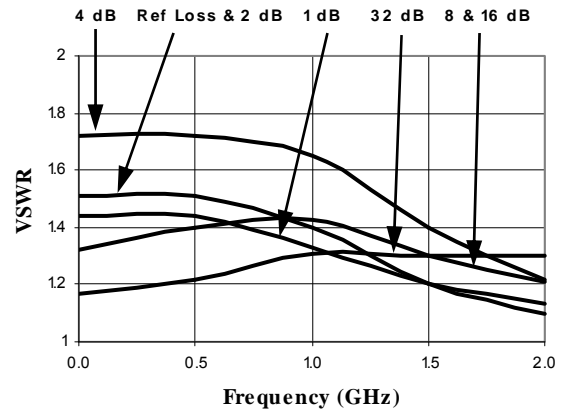


## Typical Performance Curves

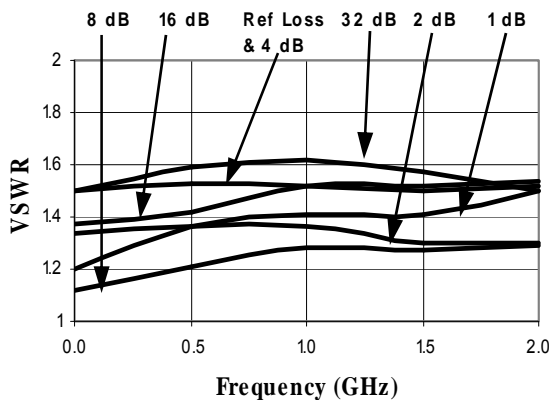
Attenuation Accuracy vs. Frequency



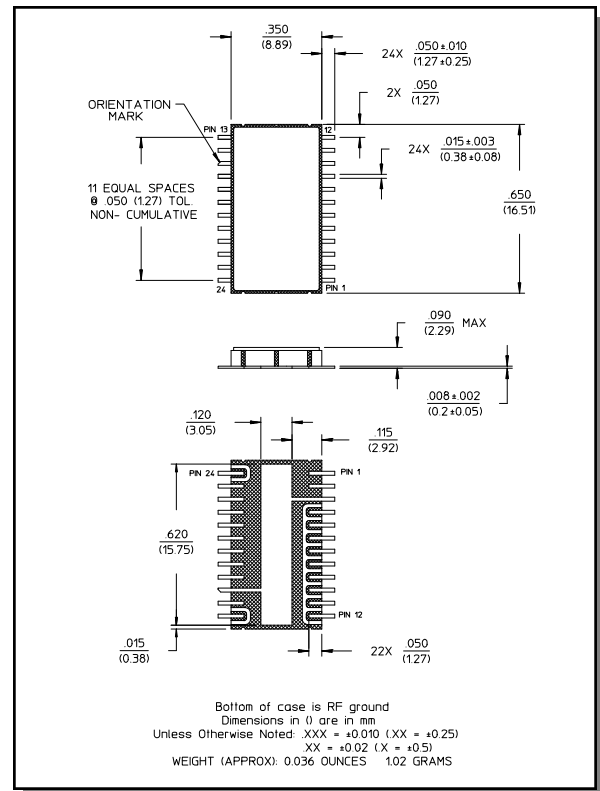
RF1 VSWR vs. Frequency



RF2 VSWR vs. Frequency



## Lead-Free, CR-13 Ceramic Package<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.